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EXPERIMENTS IN THE USE OF THE ELECTROCHEMICAL CELL
AS A BINARY MEMORY ELEMENT

by

Richard E. Hasselbring

June 2, 1965

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Report No. 180

EXPERIMENTS IN THE USE OF THE ELECTROCHEMICAL CELL
AS A BINARY MEMORY ELEMENT*

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June 2, 1965

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EXPERIMENTS IN THE USE OF THE ELECTROCHEMICAL CELL AS A BINARY MEMORY ELEMENT

Richard E. Hasselbring
Department of Electrical Engineering
University of Illinois, 1965

A read-mostly digital computer memory model is investigated using chemical cells as binary memory elements. A word-organized array of special low-charge cells is coupled to drivers and logic to form an operational regenerating memory for future study.

1. INTRODUCTION

1.1 Computer Memories

A computer is traditionally defined as a device which has the ability to perform various simple mathematical operations. Modern day automatic digital computers utilize sophisticated methods to implement this basic function. One important property of modern computers is the use of stored information to control sequenced computer operations on large amounts of stored data. The area involved in storing both the information and data is usually called the computer memory.

Most contemporary computers utilize several memory types in their design. This practice has arisen of necessity: no single memory has been invented which incorporates the necessary features which different applications require.

Many different factors determine the applicability and specific usage of a particular memory: a useful memory must be fast, compact, economical, and have high standards of reliability. Memories in use today have varying combinations of these attributes. For instance the flipflop memory is fast and reliable; however, it is not compact in comparison with other memories, and its high cost prohibits its use to specific instances where speed and reliability outweigh other considerations. Numerous other examples may be cited of general-purpose memories which fit into various categories with respect to the previous qualifications.

In addition to the broad application of general-purpose memories, increased use has been made of fixed or read-only stores for the storage of special constants or instruction sequences. Quite often the information in such a store is in the form of a connecting wire, or the physical presence or absence

of a coupling medium such as a ferromagnetic core or a fixed capacitor. Though in concept such memories are written into only once by the original manufacturer, actual practice shows that this restriction is somewhat of a hardship, particularly in prototype machines. Hence a growing trend is evident to a slightly modifiable or read-mostly store, where, though it may be difficult, writing of new information may be done under computer control, and by other than manual means. Though not necessary, it is normally true that the reduction or complete elimination of writing facilities in a memory allows other freedoms, economy and/or increased speed of reading being typical resulting advantages.

1.2 A Read-Mostly Memory Model

It is proposed to test a particular concept of a read-mostly memory using chemical cells as basic binary memory elements. The design will use the charged and discharged states of the cell to represent a binary digit. Memories of this type have been proposed using cells which can be charged to either polarity, but at present no such cells are available, at least not to the author.

Original work in the area of a chemical memory is described in the doctoral dissertation of B. Briley at the University of Illinois. He considered the basic feasibility of various chemical memory systems and the economic problems involved in an actual memory design. Dr. Briley narrowed his choice of chemistry to the nickel-cadmium system and used large Burgess cells of the CD-1 variety. Though by this method, initial feasibility of the chemical cell memory was demonstrated, the large stored charge of the CD-1 cell required the use of high-current technology generally inconsistent with the aims of high-speed memory application.

The author has been fortunate to receive some experimental Ni-Cad cells from Union Carbide which are about 1/80th the charge capacity of the CD-1 cell. This fact has reduced the cost of the circuitry by a considerable amount and made the design of a model memory a practical reality.

In contemplating the proposed memory certain basic information must be accepted from the work of others. This information is listed here in an effort to establish the context of the present investigation.

1. A high-speed chemical memory of approximation 1000 words is probably feasible.
2. The nickel-cadmium cell is the best suited cell for a chemical memory at this time.
3. No delay is contributed by a nickel-cadmium cell during read because it can be arranged to act essentially as a large coupling capacitor for the readout signal.
4. The time to fully charge a sealed, pressed-plate nickel-cadmium cell is inversely proportional to the two-thirds power of the normalized charging current.
5. A method of voltage discrimination should be used rather than a capacitance or resistance discrimination.
6. A constant current charging scheme should be used rather than a constant voltage scheme because it has been shown to be faster and to lead to fewer noise problems.¹

¹Bruce Edwin Briley. "The Electrochemical Cell as a Binary Memory Element." Report No. 144, Digital Computer Laboratory, University of Illinois, Urbana, Illinois (August 9, 1963)

1.3 Summary

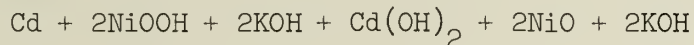
There is a definite need for a fast-access economical large-capacity storage system for today's high-speed computers. On the basis of the previous considerations it appears that the chemical cell memory might fill part of this need. The project to be undertaken here is to design a model digital memory using small Ni-Cad cells and on this basis to determine the feasibility of such a memory in terms of economics, reliability, speed and applicability.

2. CHOICE OF A CHEMICAL CELL

2.1 Introduction

The first problem confronting the designer of a chemical cell memory (Chemory or Chemicel Memory) is the choice of a cell satisfying several stringent requirements. A thorough survey made by Dr. B. Briley in 1963 showed the Ni-Cad cell to be superior to other cells then available for this application.¹ Recent communication with Professor Laitinen, Department of Chemistry, University of Illinois, and Dr. Robert Power, Director of Research, Union Carbide, shows the earlier decision to be essentially valid. These conclusions follow from several outstanding characteristics of the Ni-Cad cell.

The Ni-Cad cell is a secondary cell using nickelic hydroxide as the positive electrode, metallic cadmium for the negative electrode, and potassium hydroxide as the electrolyte. It has an average output voltage of 1.3 volts. The over-all chemical reaction can be given approximately by the following relation.²



During overcharge the Ni-Cad cells generate gas. After full charge oxygen is generated at the nickel electrode and hydrogen is generated at the cadmium electrode. In a conventional nickel cadmium battery this gas is vented through a valve. Therefore in order to seal a cell hermetically some provision must be made to control or contain excess gas.

¹Bruce Edwin Briley. "The Electrochemical Cell as a Binary Memory Element." Report No. 144, Digital Computer Laboratory, University of Illinois, Urbana, Illinois (August 9, 1963)

²Union Carbide, "Eveready" Battery Applications and Engineering Data. (The formula given is one of several probable formulas.)

This is done by the following procedure:³ the cell is constructed with excess ampere-hour capacity at the cadmium electrode. Therefore the nickel electrode will reach the full charged state before the cadmium electrode. Oxygen generation will begin but hydrogen cannot begin because the cadmium electrode has not reached full charge. The cell must be constructed so the oxygen formed can reach the metallic cadmium electrode easily. It will then react forming the equivalent of cadmium oxide. The end result is that the cadmium electrode is oxidized at a rate sufficient to offset input energy, and the cell is kept in equilibrium at full charge.

The property of hermetic sealing made possible by this process is one of the qualities which makes the Ni-Cad cell applicable to computer applications. In particular this enables one to put matrix stacks of these elements on printed-circuit cards for compact placement.

Second, the Ni-Cad cell can be recharged many times without affecting its charge capacity or efficiency to any appreciable extent.

Third, the self-discharge rate of this cell is relatively low. In fact, it is necessary to attach certain quiescent drain to the cell in the discharged state, or the cell voltage will increase to nearly a charged voltage due to internal reactions.

There are certain other facts about the Ni-Cad cell which are listed here to acquaint the reader with these properties.

1. The EMF of a cell is not a function of its size.
2. The charge capacity varies directly with the volume of active material.
3. The cycle life of a cell is not a function of its size.

³Union Carbide, op. cit.

4. Very small button-type cell packages are not yet available on the commercial market, through apparent lack of demand. Assurances have been made that an order for sufficient numbers of these cells would change this situation.⁴

In the earlier work of Dr. B. Briley, use was made of a Burgess CD-1 Ni-Cad cell having an electrical charge capacity of 20 ma hours. This cell, though adequate for the initial feasibility study of a chemical memory, was shown to severely limit the application of such a memory by virtue of the long charge and discharge times required for nondestructive cycling.

Recently with the kind assistance of Professor Laitinen, sample cells have been obtained from Dr. Powers of Union Carbide having a cell capacity of approximately .25 ma hrs, or 1/80th of that used in the original work. These sample cells are physically about the same size as the CD-1; however, technology for a reduction in physical size also seems available in the future.

2.2 Preliminary Tests

As a preliminary to the subsequent system application, several types of tests were run on the charge and discharge properties of the sample cells.

The first test consists of charging the cell to full capacity with a constant current of 1 ma, and then discharging it through a 1.2 K resistor to determine approximately a discharge curve for the cell. The result is shown in Fig. 2.1. An approximate cell charge capacity may be estimated from this curve and the value of discharging current used.

⁴Correspondence with R. A. Powers, Director of Research, Union Carbide Research Laboratory (February 25, 1965).

SPECIAL NI-CAD CELL DISCHARGED
THROUGH 1.2K RESISTOR

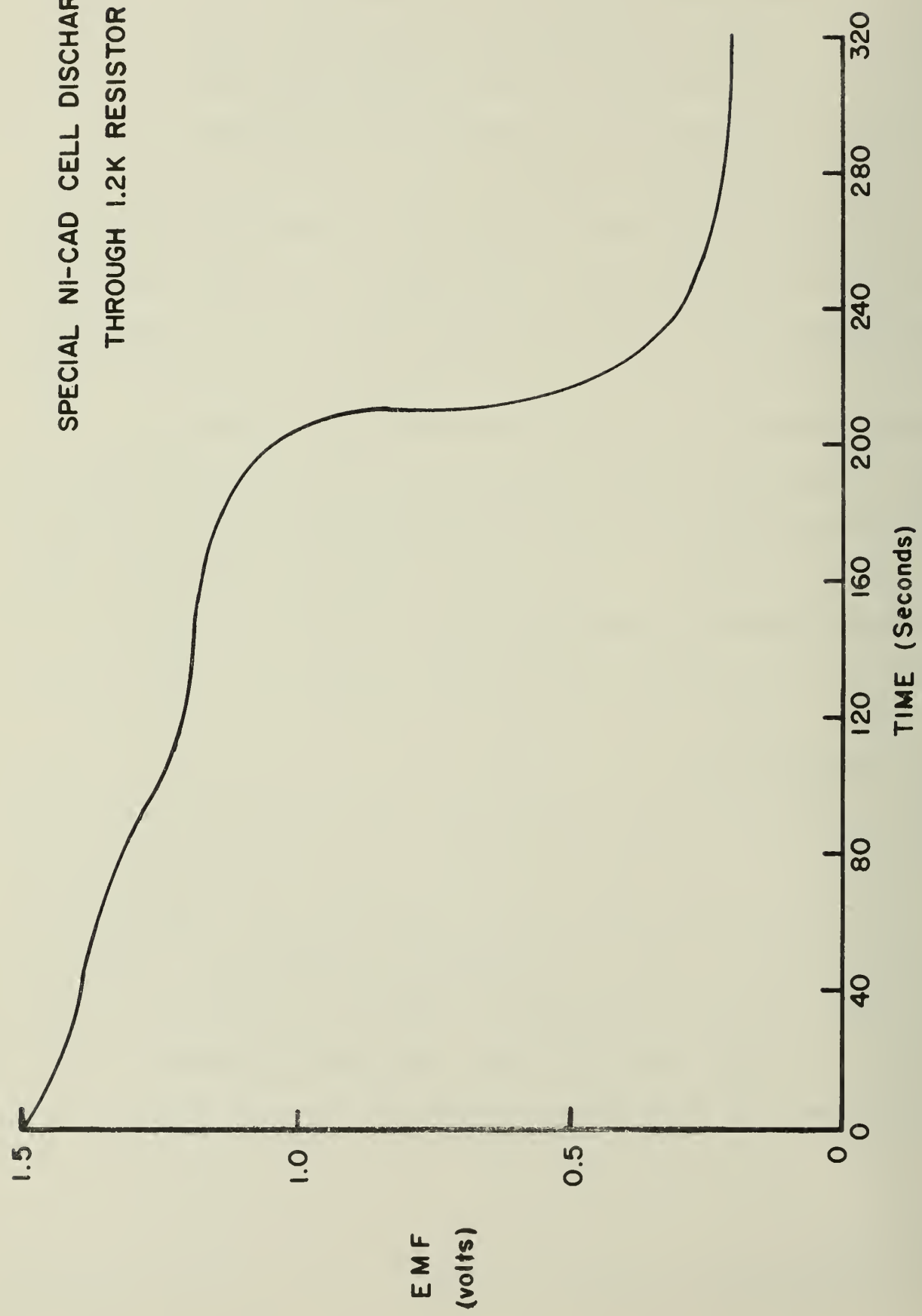


FIGURE 2.1. CELL DISCHARGE CURVE

The next test done was a maximum charging rate test performed as a sequence of higher and higher current charging and discharging cycles. The initial charging current was 10 ma and the cell was completely charged at this current. In all cases charging current was applied for a time in excess of that needed for the applied current to transport a charge equal to the approximate cell capacity. The cell was then discharged in a similar way and the process repeated with the current increased by a 10-ma increment. This procedure was terminated at a charge and discharge cycle using 100 ma. At 100 ma the charging time used was approximately 10 seconds, and there were no adverse effects on the cell. Since this current is several times greater than actual currents to be used in subsequent system design, the test was terminated with no other attempt to establish the cell's limiting capability in this respect.

At the present time tests have been set up using a chart recorder to test the long-term capabilities of the cell. This test consists of charging the cell to full charge at a specified current, disconnecting the cell for a short period and then discharging the cell at the same current. This process may be continued for a long period such that the effect on the cell's charge capacity will be established, using both the recorded data and the cell characteristics at the conclusions of the tests. This cell-life test will be done automatically using timing circuits built with relays, capacitors, etc., of straightforward design.⁵

2.3 Charging Time

By the simple definition of cell capacity, the charging time for these special .25-ma-hr cells should be given by the following formula:

⁵See Appendix B for results of test.

$$T_o = .25/I_c \text{ (Ic in ma)}$$

However, it is known that as the charging current is increased the efficiency does not remain near 100 per cent. Further it is found that it often requires even greater discharging time to ensure complete discharge. Experience shows a rule of thumb: charging time can be computed using the previous formula with a safety factor of 1.2. In the particular design to be described, system considerations led to a choice of a charge-discharge current of about 25 ma. In this case:

$$T_o = 1.2 (.25 \text{ ma hrs})/25 \text{ ma}$$

$$T_o = .012 \text{ hrs}$$

$$T_o = .012 (3600) = 43.2 \text{ secs}$$

In the design of a practical memory, T_o will be the period necessary for a write.

3. THE GENERAL MEMORY ORGANIZATION

3.1 Introduction

Before proceeding with the design of the prototype memory, ground rules are established for the design of a general memory, and the specific considerations which one must make for the Chemory are given. The memory considered for initial discussion will be of arbitrary size designated as having M-words of N-bits. Only general consideration is given to external memory environments as it is assumed that the individual designer must take this facet of the design into account, separate from the basic memory outline.

Immediately, the nature of the Chemory limits the specific environment in which it can live. In particular the charging time of the cells will generally limit the memory to a read-mostly application, which is nevertheless an important one in contemporary computer organizations. However, for a memory of this type to be generally useful the entire design must be done with a good measure of economy and emphasis on reading speed. All designs should be as simple as possible and yet consistent with the high reliability required of the general computer environment.

The selection system considered is a word-oriented type. In order to write this type of memory, M word drivers and N bit drivers will be necessary. Since the Chemory is suited for read-mostly applications no effort will be made to make the word drivers and bit drivers particularly fast. In fact, except for the question of reliability, relays could be used. However, in the application of interest, readout speed is paramount. The apparently arbitrary choice of a word-arranged selection scheme is consistent with fast readout properties.

For readout of the memory, M read drivers and N sensors will be necessary. The method to be employed here is to pull one terminal of the cell to a particular reference and to use the sensor to compare the voltage across

the cell with a second preset voltage connected to the same reference. Using the same reference in this manner insures little apparent variation of cell output with changes in the supply voltage.

The design of any digital computer memory would be of little value unless coupled with the logic circuitry necessary for an external computer connection. This design will include, therefore, a system of logic devised to allow external reading and writing of the memory, together with a method of periodically regenerating the cells while the memory is otherwise not in use.

3.2 Charge and Discharge Requirements of the Ni-Cad Cell

It is immediately obvious that one must have available a charging and discharging current at both the word selection and bit selection centers. This necessity arises from the fact that to change the state of any memory word, certain bits must be charged while others must be discharged. Further it is understood by the definition of word organization that word drivers must carry current to all of the bits in the selected word, while the bit drivers will drive only the bit in the particular selected word.

Assuming for the moment that such drivers can be built, one must find a method of isolating each cell from the rest of its neighbors, thereby preventing charge loss. This may be done by a diode selection system in which the diodes act as switches to keep the different words and bits separated. Arrangements are made to keep all diodes not in use reverse biased so that no current will flow through these paths except when it is necessary. Figure 3.1 illustrates the type of system used and shows the interconnection of diodes and drivers used in the memory design.

This system of diode selection was used first by the early designers of diode-capacitor memories. The latter memory organization and concepts are

similar to those of the Chemory except that capacitors rather than chemical cells are used to store charge. However, in the diode capacitor system, readout energies were small and transformer coupling was often used to monitor the capacitor charging currents. Such a system is thought to be unnecessary in the Chemory since the potentially large readout signals that are available seem to indicate that simple direct-coupled sense amplifiers are adequate for readout. If such is the case, obvious economic and speed advantages may result over the conventional capacitor system.

The particular methods of reverse biasing of the coupling diodes will be shown in future sections. The only major difficulty here is that certain stray leakage paths may combine to produce harmful charging or discharging of cells, an effect which obviously must be avoided.

The following abbreviations have been adopted and will be used throughout the rest of this report.

Word Write Driver Source (out)	WDO
Word Write Driver Sink (in)	WDI
Bit Write Driver Source (out)	BDO
Bit Write Driver Sink (in)	BDI
Read Driver	RD

Now that the selection system has been established, the design of each particular part will be done, and where appropriate the combination of the pieces will be shown. Before the circuit design can begin, however, there are certain other general procedures which must be considered.

Note by reference to Fig. 2.1 that currents due to leakages or the read operation should be directed so as to discharge the cell ensuring that the cell voltage remains low in the sensitive discharged state.

3.3 Components Used

A necessary preamble to a system's design is a selection of power supplies, component types, etc. An immediate problem is the size and number of power supplies which will be necessary. It seems logical to include both positive and negative supplies since both npn and pnp transistors will be used and the driver designs will be made considerably easier. The size of the voltages should be large enough to supply sufficient switching magnitudes and yet small enough to supply large current without excessive wattages. It was decided to use +5 and -5 volt supplies for the high current drivers and -10 and -15 volts for biasing and reading. The input-output levels of the memory prototype will be 0 and -5 volts.

Components were selected generally on the basis of projected price and availability. Silicon microdiodes made by Hughes were selected to help minaturize the cell matrix as much as possible. These units are fast enough to allow high-speed switching and husky enough to stand the charging current which may be necessary.

All transistors used will be of the silicon variety. Therefore all design calculations will use values appropriate to this type. The transistors used in the sensing and read-driving equipment and the diodes used generally are high-speed switching types of the kind applied extensively in the construction of ILLIAC III, the Pattern Recognition Computer, being built at the Department of Computer Science, University of Illinois, Urbana.

All designs are to be as simple as possible with the equipment at hand, since economy, being a major factor in determining the feasibility of such a memory as this, was a requirement in this study. The detailed cost of electronic components required in this system will be totaled in a cost analysis later in this paper.

Throughout the following design such things as parameter variations, power supply fluctuations, environmental changes, etc., must constantly be taken into account. The design of the writing equipment is not nearly as critical as the reading equipment, however, and therefore may be simpler and more economical.

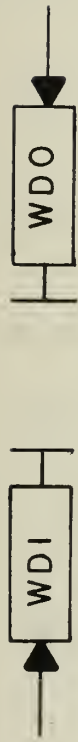
3.4 Word Write Driver Design

Several requirements for a word driver are immediately obvious. Since large currents are going to be needed, the word drivers should be constructed so that the current drain during the off state is very low. For the general reasons of closer control and expected increased life, a current limited scheme will be used to write into this memory, with a transistor used as a switch to turn the charging current on and off as needed. Recall that the driver off state must ensure that the selection diodes are back biased.

The word driver circuits chosen are shown in Fig. 3.2. Notice that in the off state the WDO diode is pulled to -10 volts while the WDI diode is pulled to +5 volts. These levels insure that the diodes will be reverse biased. Notice that the two drivers are of almost the same configuration, but with different polarity transistors.

The 10-ohm resistors in the emitter leads of the two output transistors make the circuits effectively current limited sources in the write mode. Since only one word driver can be turned on at a time, one 10-ohm resistor is common to all WDO and one 10-ohm resistor is common to all WDI. This is economical and also reduces the required space since the 10-ohm resistors must have a power rating of two watts.

The same fundamental design requirements exist for the bit drivers as did for the word drivers. The circuits chosen for the BDO and BDI are shown in Fig. 3.3. Notice that the circuits again are nearly complementary. One must



WRITE DRIVER SINK (WDI)

WRITE DRIVER SOURCE (WDO)

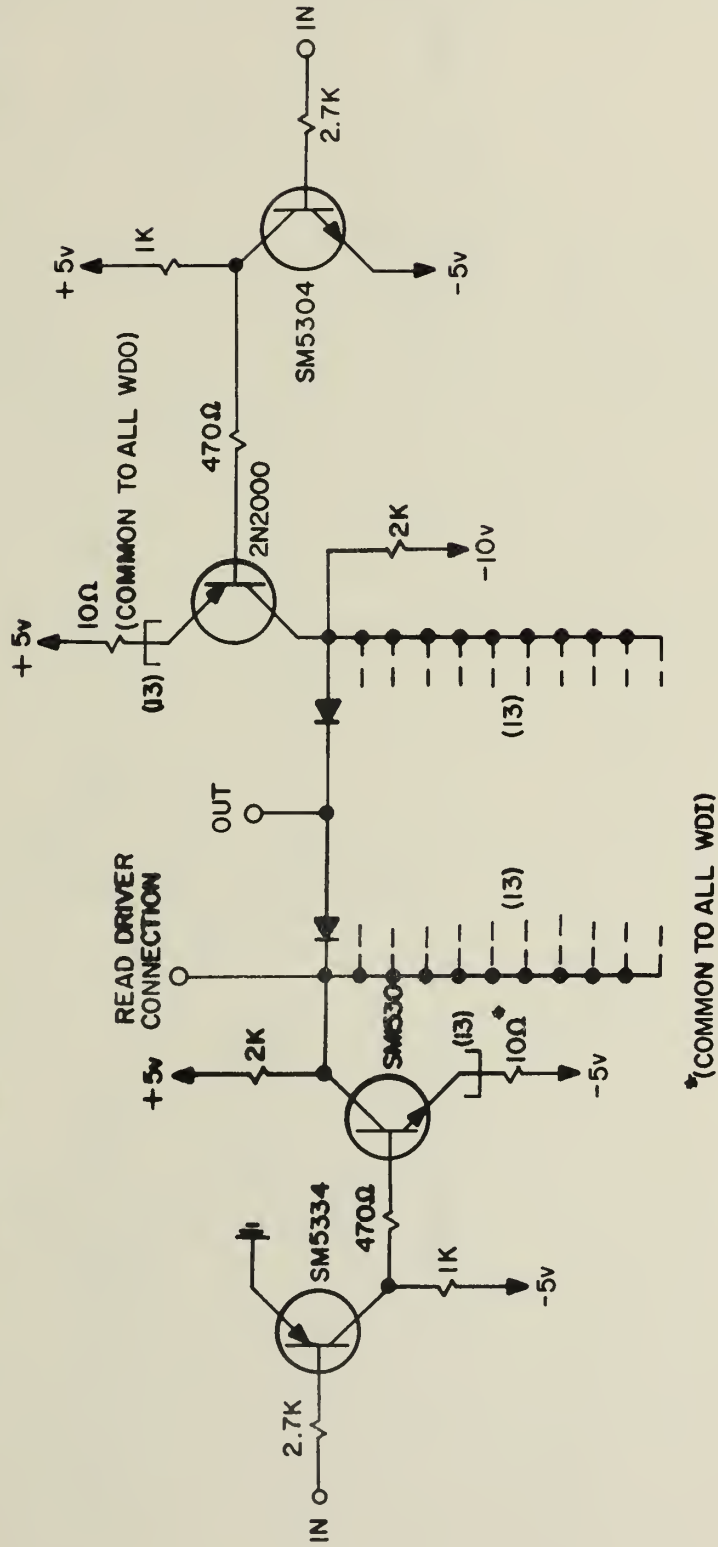


FIGURE 3.2. WORD DRIVERS

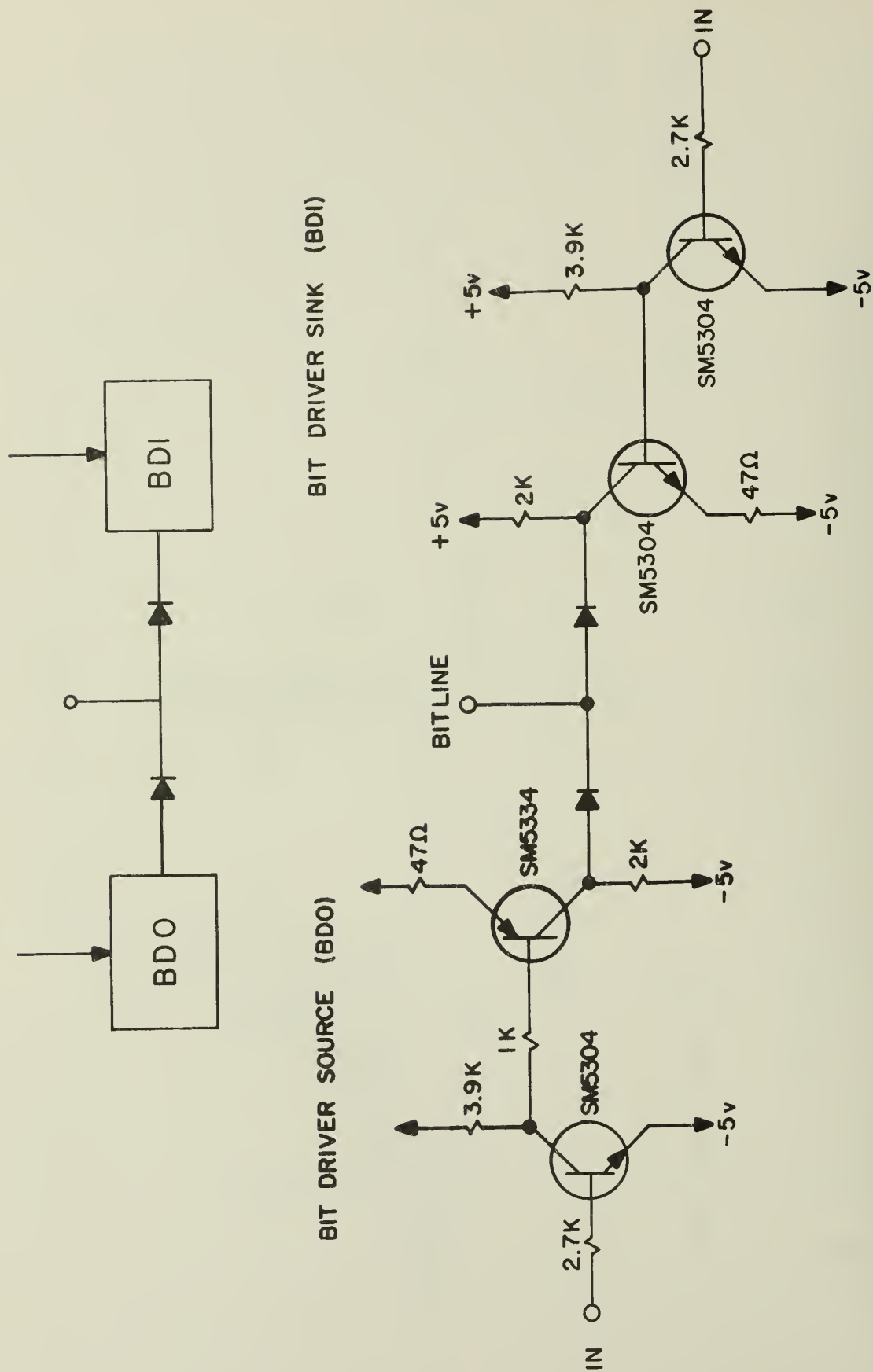


FIGURE 3.3. BIT DRIVERS

remember here, however, that while both word drivers will be turned on to write a word, only one of the bit drivers (either BDO or BDI) will be turned on for each bit line depending on whether that particular bit is to be charged or discharged.

3.5 Read Driver Design

It should be noted here that the WDI circuit could actually be used as the read driver. However, since large currents are normally used to write the memory, the resulting drivers are usually inconsistent with speed requirement, both by virtue of transistor type and current level. Therefore the decision was made to construct separate read drivers of a variety much more compatible to the high-speed readout requirements of the memory. Further effort might usefully be spent in combining the two circuits and their driving gates, though it is not considered reasonable at this time. The design that evolved is shown in Fig. 3.4.

During the rest part of the cycle the output transistor is cut off so the collector is allowed to float to whatever point is determined by the WDI. When the Read driver is actuated the transistor is saturated with V_{ce} ranging between .25 and .40 volts at a collector current of 5 to 15 ma. The particular type of transistor chosen can easily be purchased with this tolerance. The 20-pf capacitor has been added to give a high current path to the base of the output transistor providing added speed for the read operation. Notice that the transistor emitter is connected to a -10 volt supply. This will cause current to flow through the cell from two different sources during read, namely the sensor input and the BDO. The total cell current will be about 1 ma. Also, since the WDI collector resistor is connected to -10 volts, no current will flow through the 2 K resistor to the read driver. It is unfortunate that this system

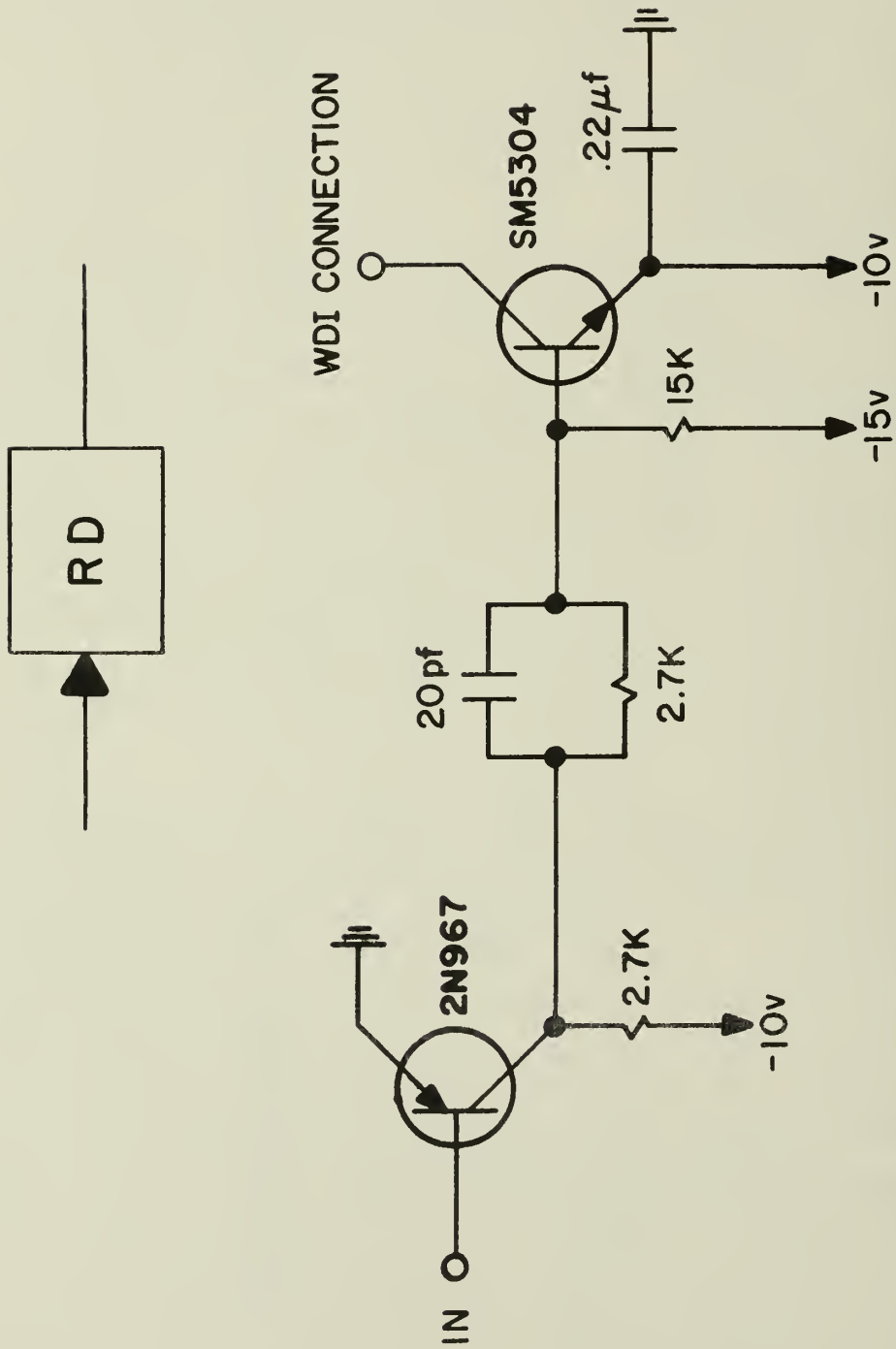


FIGURE 3.4. READ DRIVER

pulls the WDI output transistor collector to -10 volts together with the cell. Although the WDI output transistor is not terribly slow it does serve to hamper the read operation. This system could be alleviated by using separate diodes from the read driver and WDI, but the extra cost of one diode per bit is prohibitive. Finally one should notice that the input levels are again 0 and -5 volts.

3.6 Sensor Design

The design of the sensing unit is probably the most critical design of any memory system. One reason is obvious: the basic function of a memory device is the ability to remember a bit of information. However, for a memory to function usefully a system must be available whereby it can tell the outside world what it is remembering. This is then the basic job of the sensor unit: to monitor one selected memory bit when the read pulse is applied and to determine if the bit is a "1" or a "0."

The problems of designing a sensor are many, not the least of which is variation of design parameters. The experienced designer knows that it is not enough for one experimental circuit to work. The design must be such that mass-produced circuits will still fit into any sensor slot in the system.

A sensor system should be such that it will not be affected by environmental changes in the entire system, i.e., temperature variation, etc. Temperature compensation has been done partially by the reference supply shown on the left in Fig. 3.5. The two silicon junctions in the reference offset the variation of the two junctions in the read path, namely the WDI selection diode and the sensor input diode. The reference level is then controlled by the single 1 K potentiometer in the reference circuit. The actual sensor is a type of differential amplifier used as a threshold detector. It has been established

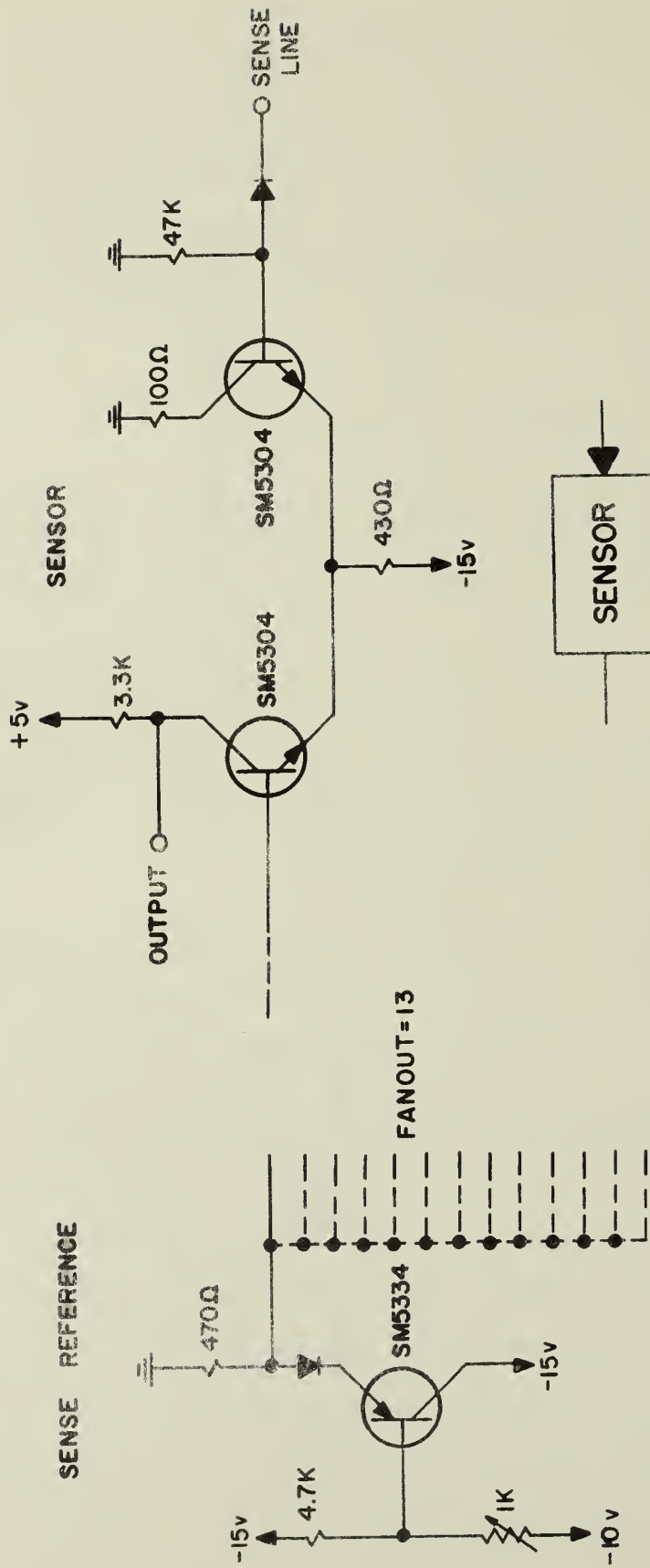


FIGURE 3.5. SENSE AMPLIFIER

that the voltage difference between the charged and discharged states of the cell will be about .6 volt. This is enough change to insure that for one state of the cell the output of the sensor will not change, that is, there will be no pulse, while in the other state there will be approximately a 5-volt pulse at the output of the sensor. This pulse is then used to drive the output logic circuitry. Notice that the output levels are again 0 and -5 volts.

The final design of the sensor is such that in fact there is a .2-volt difference required at the input to produce either 0 volts or -5 volt output. The reference supply has been built to drive more than a dozen sensors should the need arise, and it was tested by applying an additional load to the reference output.

The sensor itself was designed so that during other operations of the memory the input diode is reverse biased and the sensor does not see the write driver voltage excursions. The 47 K resistor puts a certain amount of bias current into the right-hand transistor under quiescent conditions. If the cell to be monitored is in a discharged state when the read operation takes place, the base of this transistor is pulled far enough negative to turn off the right-hand transistor and pull current through the output transistor. However, if the cell is charged, the sense line is not pulled far enough negative to forward bias the sensor selection diode and the sensor is not affected.

4.1 Introduction

In the previous chapter the design of circuitry to drive the actual memory components was given. In this chapter logic diagrams will be described to show the methods of reading, writing and periodically regenerating the memory. The logic described is given as one of many methods of solving the problem. The design is far from unique; rather its value lies in the fact that it does represent a workable method. To reduce the cost of the unit and the labor involved in construction almost all of the logic design was done using components available on printed-circuit cards at the Department of Computer Science.

The logic circuitry was designed to drive a four-word memory of 13 bits. The number of bits was chosen as 13 to correspond to external fast register connections to ILLIAC II, the large computer complex at the Department of Computer Science. Though at the present time the memory model has not been so connected, the possibilities are good that in the future ILLIAC II will be used to run further tests on the design. The number of words selected was a rather arbitrary choice. However, it did correspond to the fact that four 13-bit words could be combined to give one full 52-bit ILLIAC II word.

The first step involved in the design of the logic was to outline exactly what would happen in each of the three modes of memory operation. These modes are: Read, Write and Periodic Regeneration (henceforth designated as PR). A system was then designed in which each of these procedures could occur separately and yet be interconnected so that each is dependent on the other two.

4.2 Reading the Memory

There will follow in succeeding paragraphs an attempt to list the various procedures which must occur for an external read cycle to be completed.

It is assumed at this point that the logic will receive an address and a read pulse from an external source. The first step is then to gate the address into an address register. The decoded address register output coupled with the read pulse will then actuate the read driver circuitry for the correct word (see previous chapter). The read pulse will also form a strobing signal. This signal will be used to gate the output of the sensing units into the data register. A delayed pulse will gate out the information in the data register to the external computer environment.

One must take into account at this point the fact that the logic circuitry is arranged to be regenerating during idle periods and therefore normally will be performing PR when the read pulse arrives. Therefore additional logic circuitry must be included which allows the read pulse to turn off PR, complete the read cycle and then allow PR to begin again on the same word. The method of doing this will become clearer in later sections of this chapter.

4.3 Writing the Memory

At this point we again assume that a write pulse and an address are received from the external unit. The address is gated into the address register and the bits of information to be written are gated into the data register. At the same time PR is stopped by the incoming pulse. The decoder coupled with the write pulse then turns on the appropriate word drivers. A decoder is also used to turn on gates from the data register which actuate the correct bit drivers (i.e., "1" or "0"). The drivers are then held on for a period of time which insures proper charging of the cells. At the completion of cell charge, a pulse is formed which restarts the PR scheme.

4.4 Periodic Regeneration

We will assume initially that PR can make use of much of the same circuitry used in the read and write modes. This circuitry will then be coupled with the necessary added hardware to make regeneration possible.

The operational order involved in the PR will be outlined here. Let us assume for the moment that we have formed a regeneration signal. We must then read the contents of the word to be regenerated and put this information into the data register. When this subcycle is completed we actuate the write driver circuitry and write the cells to the same state from which we read the previous information. When the write period is completed a pulse appears signifying that the PR cycle has been completed. The next word is accessed and the cycle begins again. A counter is included whose function it is to cycle through all words of the memory and thus allow the periodic regeneration scheme to continue indefinitely. Recall that in a previous chapter it was stated that the cells were internally protected from overcharge so that no problem of excessive charge should occur.

One must also take into account that at any time during the previous sequence of events a read or write pulse could arrive. Therefore, the control circuitry must be able to cope with several different types of operating sequences. There are actually only four situations to consider. The first situation is a read pulse arriving at the memory system while the PR scheme is reading a word for its own use. The second situation corresponds to a write pulse arriving during PR read. The third case is a read pulse arriving during PR write, and the fourth case is a write pulse arriving during PR write. These situations will be checked when more of the initial design has been described.

One might also include a system where the computer is informed that the memory has gone too long without a total periodic regeneration; however, this frill is not included in the present prototype design.

Finally in the application of this system to a larger memory of M words, provisions must be made to account for the total regeneration of the memory. Assume T_p is the time for a PR cycle. Then $(M)(T_p)$ equals the time necessary for total regeneration. If this time would exceed the minimum time a cell could operate without regeneration the system will not work. This product must be considerably less than the cell charge decay period in a practical memory to guarantee a reasonable number of read cycles per regeneration.

To determine the minimum time between regeneration, several factors must be considered. One is the self-discharge rate of the cell. It has been shown for the CD-1 Burgess cell that the self-discharge rate is about 20 per cent per year. Therefore, it is permissible to neglect it in the following discussion.

Second, the charge is depleted by stray paths which allow small amounts of current to discharge the cell. Specifically this current leaks through the coupling diodes. Assuming that the diodes are high quality silicon diodes, the leakage can be neglected. Notice that the leakage that does appear discharges the cell rather than charging it.

To compute the charge loss due to a read, a read pulse width of 50 nanoseconds is assumed. The cell current is approximately 1 ma. Therefore, the charge loss during one read is approximately $(1 \text{ ma}) \cdot (50 \cdot 10^{-19})$
 $= 50 \cdot 10^{-12}$ coulombs. Assuming a 4-mc read rate, it would take approximately 52 hours to deplete the cell charge to approximately 75 per cent of its full charge.

Certain approximations have been made in the previous paragraphs; however, the methods employed are general and the 52 hour figure does show that the system is feasible in this respect.

4.5 Actual Logic

The reader is now referred to the logic diagram in Fig. 4.1, where the system shown is an implementation of the discussion given in the preceding sections. An attempt will be made to explain why only certain of the particular logic boxes were used, and the reader is asked to refer to Appendix A for a further discussion of the more nebulous logic symbols and detailed circuits. Certain parts of the design will need no explanation, while others are unique to this design and will be expanded upon slightly.

While the memory has really only three states, three individual two-state devices were used to control the three separate functions. This was done to simplify much of the design. One flipflop was used to control the read cycle, a second to control the write cycle, and a third to control PR. A data register was constructed using 13 flipflops and the required input-output gates. Single-side gating was used to reduce the amount of necessary circuitry; however, double gating would probably be used in an application where speed was of primary interest. An address register was constructed using two flipflops since only four words will be used in the proposed sample memory. A simple decoder selected the word corresponding to the contents of the address register. The outputs of the decoder are then fed through multigated circuits to the appropriate read and write drivers. Single gating was again used for the counter input and separately for the external address inputs to the address register.

The counter is controlled by the output of the regeneration oscillator. This oscillator has a period equal to twice the period necessary for regeneration. In this case the period was about 40 seconds. The additional time not needed for regeneration was approximately 20 seconds. Since we have assumed previously that this memory is by necessity a read-mostly memory, we will assume at this point that during normal operation only read cycles will interrupt the PR cycles. Assuming that a read cycle takes approximately 250 nanoseconds and that periodic

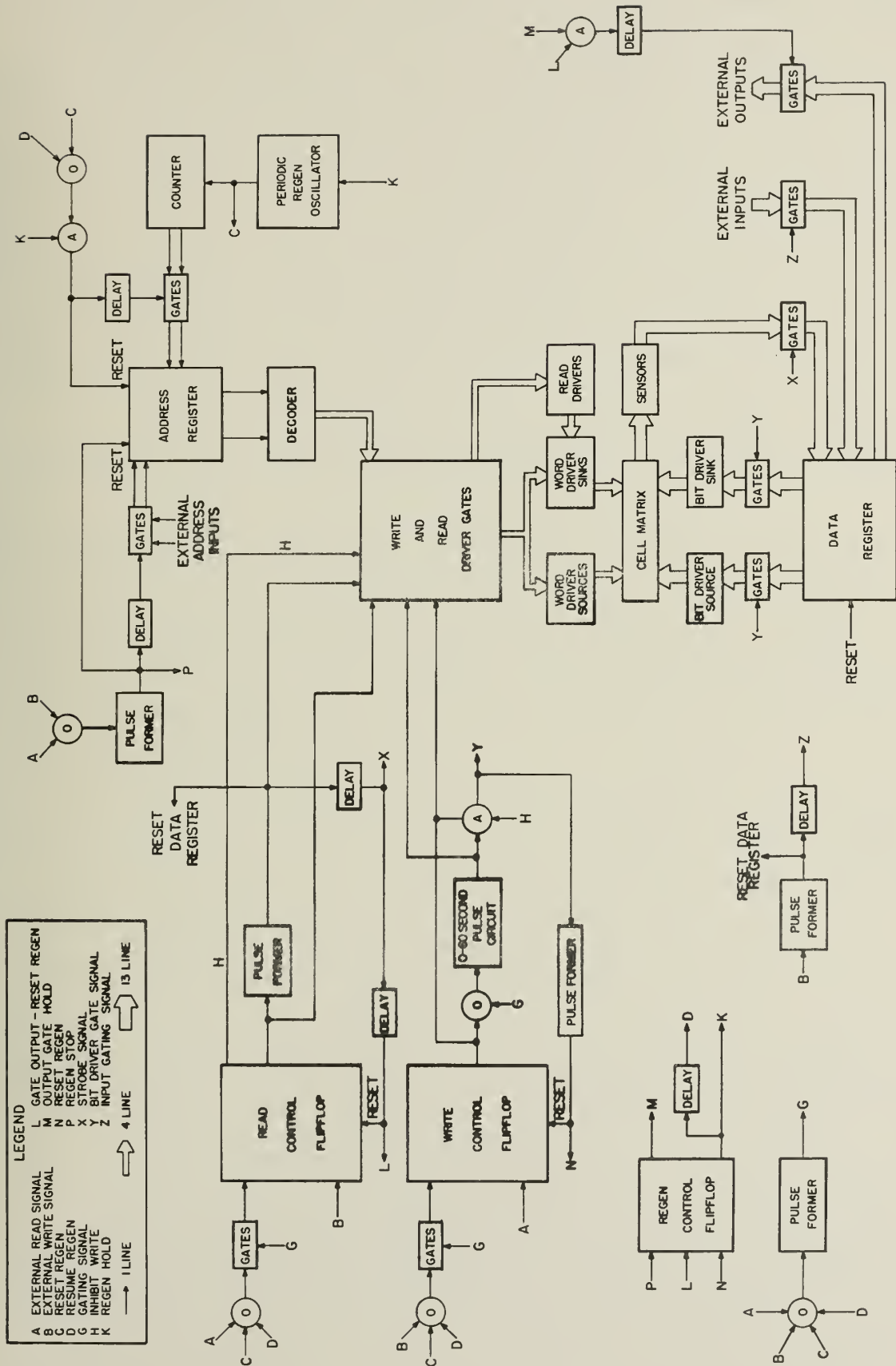


FIGURE 4.1. LOGIC DIAGRAM FOR CHEMICAL MEMORY

regeneration can begin in another 500 nanoseconds, we complete an external read intrusion in 750 nanoseconds. During each 60-second time interval, only 40 seconds are necessary for writing the word. This leaves 20 seconds for external reads which leads to a maximum figure of 27 million reads during an oscillator cycle for full regeneration to be guaranteed.

The regeneration problem must certainly be taken into account by any systems designer wishing to use such a memory. If more than this maximum number of reads would be necessary from the memory in a 60-second period, the oscillator cycle could be increased. It is certainly also possible to use a system where PR is turned off during part of the day and does its work other times.

Particular attention should be paid to the pulse-forming network which forms the G signal. This signal is a 100-nanosecond pulse used to gate various functions throughout the logic pattern. Notice that it has four inputs corresponding respectively to a read input pulse (A), a write input pulse (B), a completion of regeneration pulse (C) and a continue regeneration pulse (D). Accordingly a pulse is formed at four different times corresponding to the four individual actions with which we are concerned.

The reader's attention is now drawn to the input circuit of the read control. Three different inputs can gate the read control to read. These inputs occur: (1) when a read pulse arrives, (2) when a regeneration cycle is completed or an external cycle is completed, and (3) regeneration is to begin anew on the same word. Notice also that the same inputs except for the external one are used to set the write control. The system used here is as follows: when a read or write pulse arrives at the memory the appropriate control box is turned on while the other control box and the regeneration box are turned off. At the completion of the appropriate cycle the regeneration control is then turned on and the pulse denoted D turns on both the read and write control. An inhibit line (H) from

the read control stops the write circuitry from turning on until the read cycle has been completed. When the read cycle is completed, write begins and PR continues as it did before the external pulse arrived. At the completion of a regeneration cycle the pulse denoted C gates on the read and write controls, advances the counter, and gates the address register. It becomes apparent here that D must also gate the address register from the regeneration counter since the register contents were changed by the external order previously obeyed. It should be noted here that C and D are short pulses and not dc levels.

Throughout the diagram various delay symbols are shown. These delays were necessary in order to allow the sequencing of events. The time of the various delays were dependent on the type of circuitry which a system designer would use in his particular application, and therefore actual delays are given only parenthetically. The read logic generates a pulse which is used to actuate the read driving circuitry. It is probable that this pulse must be as short as possible to allow accurate reading.

Checking the earlier considerations, one sees that one now has a system which will handle any of the four special sequences which would occur during PR. In particular this system allows either a read pulse or a write pulse to turn off periodic regeneration which can be in either its read or write state, complete the needed cycle and turn periodic regeneration back on. It is acknowledged that an external write pulse could upset the charging of the particular word which is being recharged. This fact is acceptable, however, due to the fact that the memory is a read-mostly memory!

This completes the initial discussion of the logic diagram. The reader is again urged to check Appendix A for further discussions of individual logic designs. Certain other circuitry problems do arise when one attempts to build

such a system. However, a discussion of these problems will not be attempted in this paper, and it will suffice to say that the logic system discussed here has been built and operated.

5. COST ANALYSIS

In the following sections a cost analysis is done to give a rough idea of the cost per bit of a chemical cell memory. In the first section an M-word, N-bit memory is proposed and all costs evaluated with this in mind. In this case it is assumed that the number of bits will be small enough that the available word and read drivers will drive all the bits per word. This allows computation of costs using the circuits designed in this paper.

In the case stated the following circuits would be necessary:

1. M word driver sources
2. M word driver sinks
3. M read drivers
4. N sensors (also one sense reference)
5. N bit driver sources
6. N bit driver sinks
7. $2MN$ coupling diodes (assuming the word drivers use none)

The use of existing circuits leads to the following needs in hardware:

1. $4M + 6N$ switching transistors
2. $2M$ medium power transistors (600 mw)
3. $2MN + 2N$ microdiodes = $2N (M + 1)$
4. $10N + 5M$ resistors
5. $2N$ capacitors

The following costs of hardware were used in this cost analysis:

Switching transistors	\$0.50
Power transistors	0.75
Microdiodes	0.25
Resistors (two per cent metal film)	0.05
Capacitors	0.15

This led to a cost per bit of the basic memory hardware of:

$$\text{Cost/Bit} = \frac{(4M + 6N)(.50) + 2M(.75) + (2MN + 2N)(.25) + (10N + 5M)(.05) + 2N(.15)}{NM}$$

$$= (3.75M + 4.30N + .50MN)/MN = \frac{3.75}{N} + \frac{4.30}{M} + .50 \text{ excluding the cell cost.}$$

We see here that if we had an array of infinite size the circuit cost would approach \$0.50 per bit. This base cost is due to the two coupling diodes in the word line and is obviously the limiting factor in an economic analysis of this sort. In the case of a 100-word 13-bit memory the cost per bit would be \$0.83 per bit for the basic matrix and hardware except for the cells. No cost has been determined for the basic cells except for corresponding prices of much larger cells. This cost, however, will simply add directly to the earlier computed cost per bit.

An attempt will be made here to compare the cost of the projected chemical memory to a magnetic core memory of approximately the same size. Several assumptions will be made concerning future costs of items using the cost changes of the past five years. It is entirely feasible that the cost of micro-diodes could decrease to \$0.10 per diode in future years. In large quantities it is feasible that the Ni-Cad cells could be manufactured for as little as \$0.30 per cell. Thus the basic cost is approximately \$0.50 per bit. For the associated driver and sensing units listed earlier, the approximate cost is about \$0.20. An additional 2M gates will be necessary in the logic circuitry to perform the reading and writing operations, and this will add approximately \$0.05 per bit. If one allows an additional \$0.20 per bit due to the necessary logic circuitry, then a figure of \$0.95 per bit is not a bad estimate for the basic electronic hardware. However, there are other considerations which must be taken into account at this time.

The cost of the matrix stacking on printed-circuit cards and the labor involved in the construction of this memory must be considered. The size of the

experimental cells used in this experiment prohibits close packing, but the author has been assured that if there were sufficient demands for these cells, they could be manufactured in a much smaller package. This coupled with the use of microdiodes would allow close spacing the matrix on printed-circuit boards, and in turn allow the mass production of a cell stack and cut down on the construction costs. A printed-circuit card would cost about \$4.50 for material and construction. This leads to a cost per bit of about \$0.09 (assuming four words per card). Allow another \$.03 per bit for card racks and wiring and the total cost comes to \$1.07 per bit.

However, when one does a feasibility check, many other things besides cost must be considered. Does the memory have some other advantages which might make it worthwhile to invest the added cost? The advantages of the chemical memory lie almost entirely in the fact that read can be accomplished very quickly and that computer-controlled writing, though difficult, is available. The only delay which one must encounter is the delay associated with the diodes coupling the read driver with the cell and the cell with the sensor. In practice other delays are also inherent in a design of this type. The only real deterrent to high-speed read is the speed of the available circuitry used to drive the read circuitry and propagation in the cell array and wiring. Mentioned earlier is the fact that the cell itself acts as a large coupling capacitor during read. Therefore it adds no appreciable delay. Delay is incurred in the logic circuitry where the pulses must be of a sufficient duration to allow sequencing of events and to ensure full up and down conditions when the inherent delay of the logic circuitry and driver is taken into account. Therefore, if faster methods of performing the actual logic functions are used or if the actual circuitry used to do this is improved, the pulse widths could be shortened and the over-all read cycle time could be reduced considerably.

6. CONCLUSION

The purpose of this study was to investigate the use of the Ni-Cad cell as a binary memory element. This was accomplished by first testing the cell and then designing the external equipment necessary to make the charge storage phenomenon compatible with a computer environment.

Although the cost of the system may be prohibitive for some applications at the present time, the feasibility of the system is obvious. The readout speed of the memory is dependent only on the external circuitry, which indicates that future improvement in circuit speed and organization could make the memory quite fast.

Assuming that smaller cells are available, the system could certainly be made small enough to make it practical for normal ground-based uses.

Apparently, in addition, the reliability of the system is limited only by the properties of the cell and can be made satisfactorily high.

BIBLIOGRAPHY

1. Briley, Bruce Edwin. "The Electrochemical Cell as a Binary Memory Element." Report No. 144, Digital Computer Laboratory, University of Illinois, Urbana, Illinois (August 9, 1963).
2. Union Carbide, "Eveready" Battery Applications and Engineering Data.
3. Rajchman, Jan A. "Computer Memories--A Survey of the State of the Art," Proc. IRE, Vol. 49, No. 1 (January 1961).
4. Babb, Daniel S. Pulse Circuits Switching and Shaping. Prentice Hall: Englewood Cliffs, New Jersey, 1964.
5. Yovits, Marshall C. Large Capacity Memory Techniques for Computing Systems. The McMillan Company: New York, 1962.
6. Smith, Charles V. L. Electronic Digital Computers. McGraw-Hill: New York, 1959.
7. Flores, Ivan. Computer Logic. Prentice Hall: Englewood Cliffs, New Jersey, 1960.

This Appendix has been added to clarify certain parts of the logic design which were not obvious in the earlier treatment of this subject. The author wishes to cover five basic circuits which were used in the design.

These five circuits are the following:

1. Time-Delay Circuits
2. Pulse-Forming Networks
3. 0 to 60-Second Delay
4. Write and Read Driver Gating Systems
5. Standard NOR Circuit

A.1 Time-Delay Circuits

In the logic design various delay circuits were necessary to allow for the correct sequencing of events. The delays necessary varied in length from 20 nanoseconds to 100 nanoseconds. These delays were constructed by two different methods depending on the amount of delay necessary. For the shorter delays the time delay of a simple NOR circuit or combination of NOR circuits was used. As the delays increased in length, however, it became necessary to use artificial delay lines. Since these delay lines were available on printed-circuit cards, they were used wherever necessary. In actual practice where more strict time conditions would be imposed it would be proper to build delay circuits which more nearly correspond to the delays necessary. (Since NOR circuitry was used throughout the construction of this design, some extra time delay was incurred in obtaining the correct pulse polarity.)

A.2 Pulse-Forming Circuits

The logic diagram shown in Fig. 4.1 has various pulse-forming networks included in it. Figure A.1 shows the type of network used for these pulse formers. The delay symbol shown is made up of a delay line and its input-output circuitry. The symbol delta (Δ) is used to represent the delay time of the line.

One should notice that this network forms a positive output pulse of delta duration when the input goes negative and no pulse whatsoever when it goes positive. The network then functions as a single-shot circuit which forms a pulse at the trailing edge of a positive input pulse. It is very handy to use this form of network to generate a pulse at the completion of a cycle, and it is used this way in most cases. In the case of the G-forming network, however, it is simply used to form a pulse of the necessary duration.

A.3 0 to 60-Second Pulse Circuit

Two circuits of the type illustrated in Fig. A.2 were used in this logic design. The circuits have the property that when the input was actuated by a pulse of finite length, the output goes up immediately and stays up for a time specified by an external capacitor. The term finite is emphasized here because during the construction of the circuitry it was realized that the width of the input pulse necessary to fire the circuit varied with the length of the output pulse desired, a fact which should have been obvious sooner.

One of these circuits was used to control the length of the write cycle time, while the other controlled the period of the PR oscillator. Since the circuit was equipped with a potentiometer to partially control the output pulse width some amount of balancing could be done after the final wiring was completed.

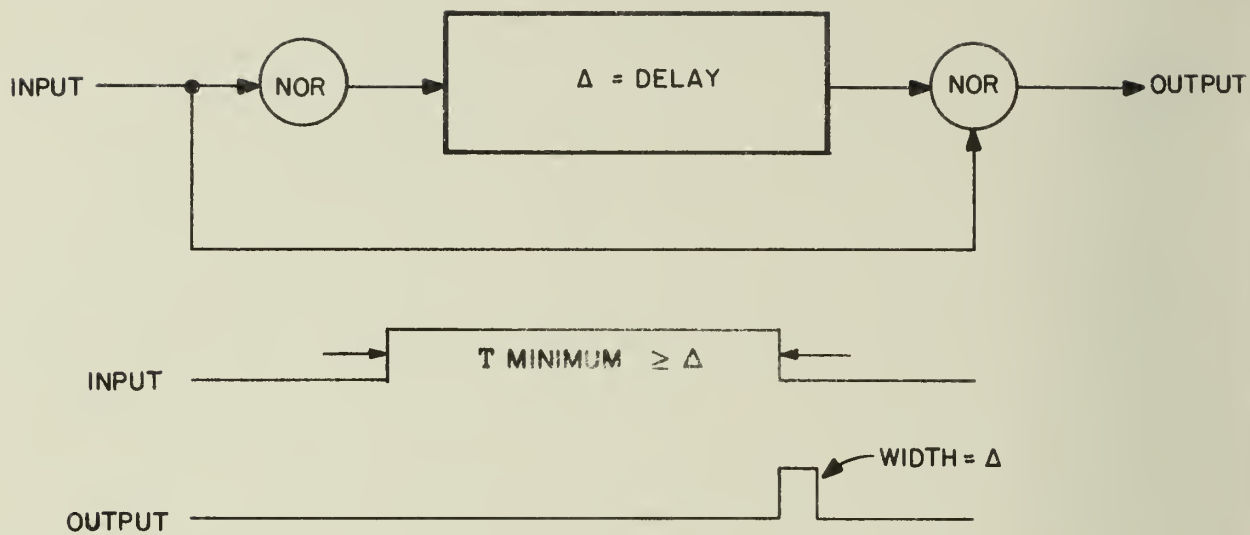


FIGURE A.1. PULSE-FORMING CIRCUIT

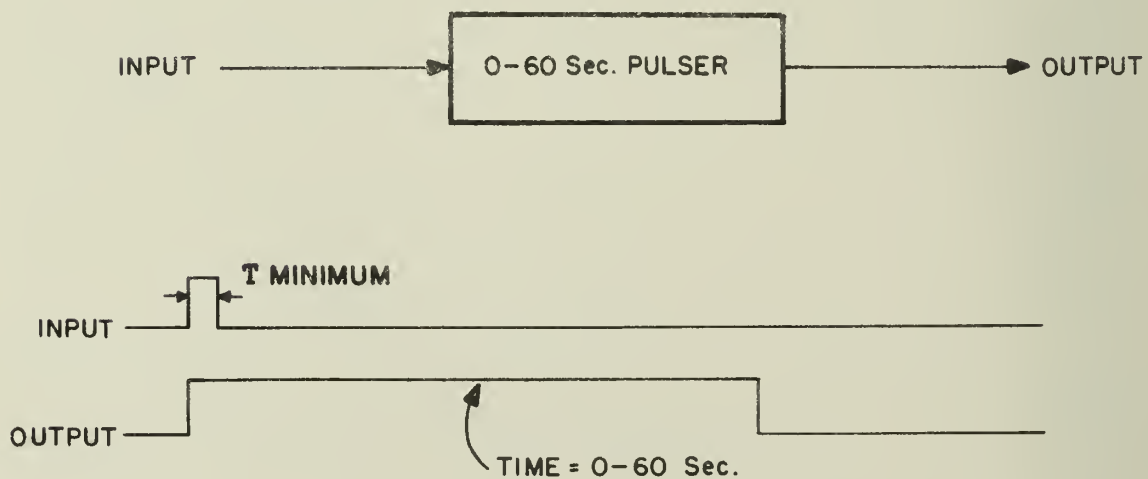


FIGURE A.2. 0 TO 60-SECOND PULSE CIRCUIT

A.4 Write and Read Driver Gating Systems

The illustrations in Fig. A.3 show the actual realization of the read and write driver gating systems. The various connections to the gates are shown on the basic logic diagram in an earlier chapter.

A.5 Standard NOR Circuits

The circuit shown in Fig. A.4 is the standard NOR circuit used as the basic building block in the construction of the logic circuitry.

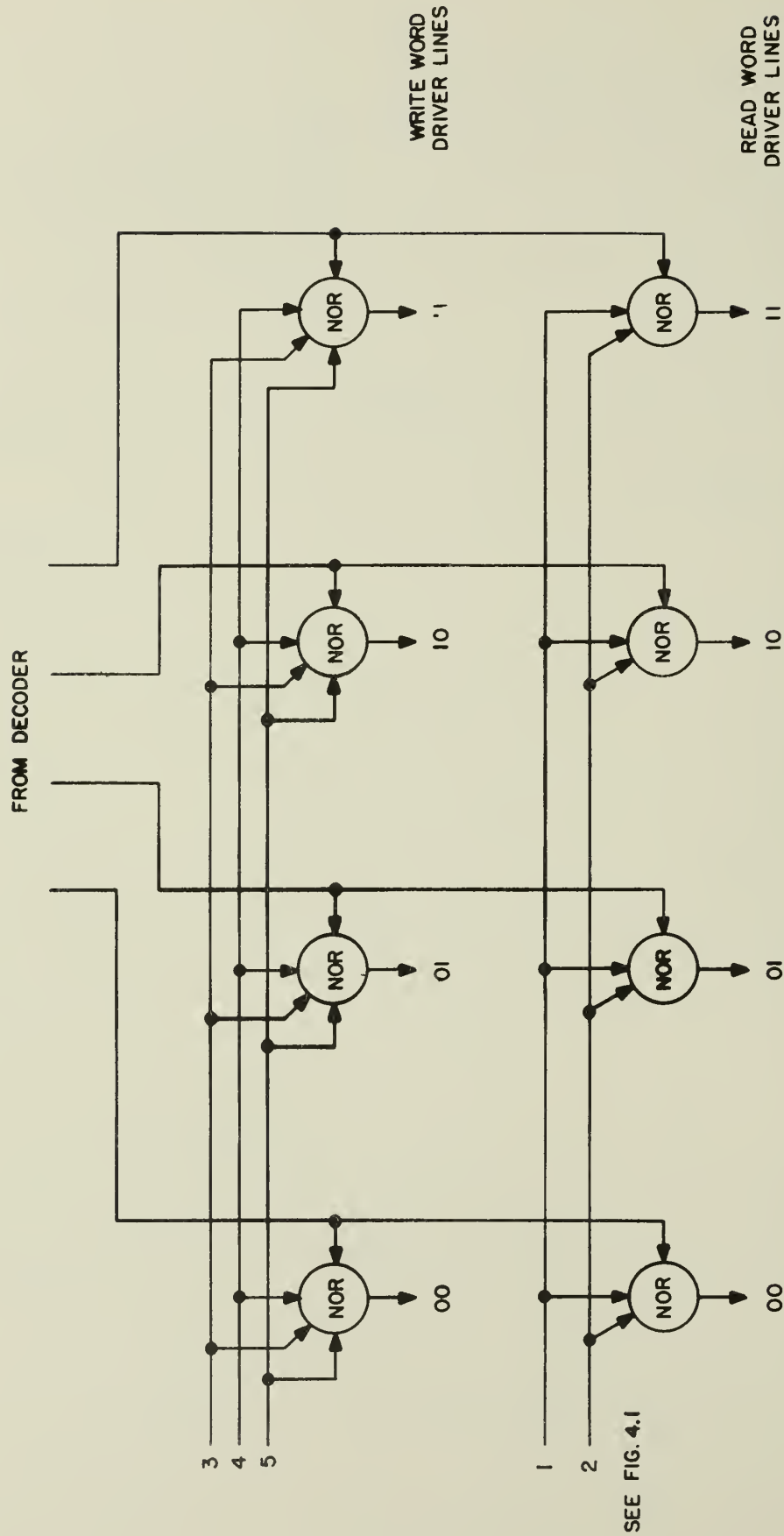


FIGURE A. 3. WRITE AND READ DRIVER GATING SYSTEMS

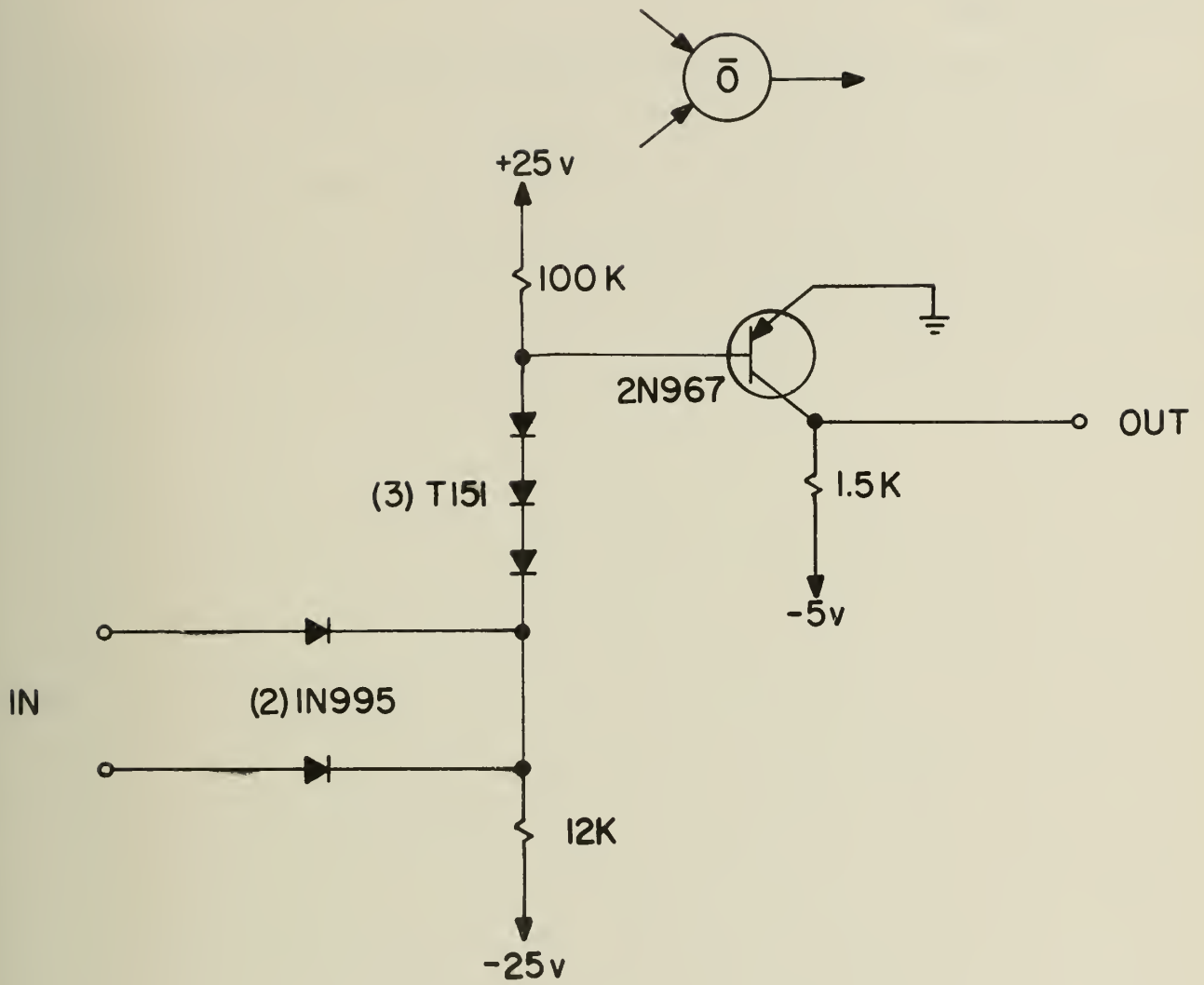


FIGURE A.4. STANDARD NOR CIRCUIT

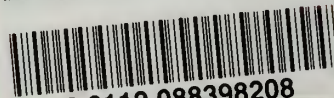
In Chapter 2 of this paper reference was made to a cell test of long duration. At the completion of this paper the test had been in operation for a period of one week.

Recall that the test involved alternately charging the cell and then discharging it with a specified current. The current was chosen to be 50 ma to accelerate the life test and the time per half cycle was chosen to be 30 seconds.

At this time no measurable damage has been done to the cell and no noticeable heating has occurred. The test will be continued for a much longer time, however, to check the long-term durability of the cell.



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